REMARKS

The Examiner's Office Action of June 20, 2003 has been received and its contents reviewed. Applicants would like to thank the Examiner for the consideratio given to the above-identified application.

Claims 1-10 are pending for consideration, of which claims 1-3, 6-7 and 10 are independent. By this Amendment, claims 1-3 and 7 have been amended. Accordingly, In view of these actions and the following remarks, reconsideration of this application is now requested.

Referring now to the detailed Office Action, Claims 6 and 10 stand objected to as dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In response, Applicants respectfully submit that claims 6 and 10 have already been amended as independent in the Amendment of March 24, 2003. Hence, no further amendment to claims 6 and 10 at this point should be necessary.

Claims 1, and 3-5 stand rejected under 35 U.S.C. §103(a) as unpatentable over Agarwal (U.S. Patent No. 6,218,256 – hereafter Agarwal '256) in view of Agarwal (U.S. Patent No. 6,465,828 hereafter Agarwal '828) further in view of Ouellet (U.S. Patent No. 5,747,361). Further, claims 2, 7-9 stand rejected under 35 U.S.C. §103(a) as unpatentable over Nagasaka et al. (U.S. Patent No. 5,973,408 – hereafter Nagasaka) in view of Ito et al. (U.S. Patent No. 5,561,326 – hereafter Ito). These rejections are traversed at least for the reasons provided below.

Amended independent claims 1, 2, 3 and 7 of the present invention relate to a gate electrode structure including a silicon-containing film containing silicon as a principal constituent, a barrier metal layer formed on the silicon-containing film and a metal film with a high melting point formed on the barrier metal layer, and a method for fabricating the gate electrode structure.

Conventionally, if a barrier film is composed of titanium nitride (TiN), nitrogen in the barrier film reacts with the silicon in a polysilicon film to form a reaction layer composed of a silicon nitride (SiN) film at the interface, and the interface resistance becomes higher. In consideration of this conventional problem, an object of the invention is lowering the

interface resistance between a silicon-containing film and a metal film with a high melting point included in a gate electrode structure.

According to the invention recited in the amended claims 1 and 3, the barrier metal layer of the titanium nitride rich titanium as compared with the stoichiometric ratio is formed between the silicon-containing film and the metal film with a high melting point, and therefore, the amount of nitrogen included in the barrier metal layer is small. Accordingly, since the barrier metal layer includes a small amount of nitrogen to be reacted with silicon of the silicon-containing film through high temperature annealing of the gate electrode structure, a reaction layer of a compound principally including silicon and nitrogen is never formed or is formed in merely a small thickness between the barrier metal layer and the silicon-containing film. As a result, even when the gate electrode structure is subjected to high temperature annealing, the interface resistance between the silicon-containing film and the barrier metal layer can be prevented from increasing, and therefore the interface resistance between the silicon-containing film and the metal film with a high melting point can be prevented from increasing.

According to amended claims 2 and 7, since the first barrier metal layer of the titanium nitride rich in titanium as compared with the stoichiometric ratio is formed on the silicon-containing film, the amount of nitrogen reacted with silicon of the silicon-containing film through high temperature annealing of the gate electrode structure is small. Therefore, a reaction layer of a compound principally including silicon and nitrogen is never formed or is formed in merely a small thickness between the first barrier metal layer and the silicon-containing film. Accordingly, even when the gate electrode structure is subjected to high temperature annealing, the interface resistance between the silicon-containing film and the first barrier metal layer can be prevented from increasing, and therefore the interface resistance between the silicon-containing film and the metal film with a high melting point can be prevented from increasing.

Furthermore, since the first barrier metal layer and the second barrier metal layer, in which nitrogen composite is higher than the stoichiometric ratio, are disposed between the metal film with a high melting point, a dopant introduced into the silicon-containing film is prevented from moving by the first barrier metal layer and the second barrier metal layer, and hence is prevented from diffusing into the metal film with a high melting point.

Further, a silicide layer of the metal with a high melting point can be avoided from being formed through a reaction between silicon of the silicon-containing film and the metal with a high melting point of the metal film, such as recited in independent claims 6 and 10.

Turning now to Agarwal '256, this reference teaches an invention that relates to an electrode and a capacitor structure for DRAM, in which it is disclosed that a lower electrode (12) composed of HSG poly-silicon film is formed on a substrate (10), a dielectric layer (14) composed of Ta_2O_5 is formed over the lower electrode (12), a barrier metal layer (l6) composed of TiN is formed in an oxygen saturated state, and an upper electrode (18) composed of a metal film with a high melting point is formed on the barrier metal layer (16). Thus, the electrode structure formed on the dielectric layer (l4) includes the barrier metal layer (16) and the metal layer, which has a high melting point and composed of the upper electrode (18), but not poly-silicon film composed of the lower electrode (12). Moreover, the barrier metal layer (16) is an oxygen-rich TiN layer.

On the other hand, the gate electrode structure of claims 1 and 3 of the present application is formed on the gate insulating film and composed of the silicon-containing film.

Applicants respectfully submit that while the silicon-containing film recited in claims 1 and 3 is formed on the insulating film disclosed, in Agarwal this film is formed under the insulating film. In other words, the arrangement of the gate electrode structure in claims 1 and 3 is opposite to that of Agarwal '256. Moreover, the barrier metal layer recited in claims 1 and 3 of the present invention is a Ti-rich TiN film. Therefore, the gate electrode structure in claims 1 and 3 is clearly distinguished from that of Agarwal '256 in view of the structure and film composition of the barrier metal layer.

Turning now to Agarwal '826, this reference discloses an electrode and capacitor for DRAM, in which, as illustrated in Fig. 4A, a lower electrode (350) is formed on a through contact (340), a diffusion barrier layer (355) is formed on the lower electrode (350), a dielectric layer (360) is formed on the diffusion barrier layer (355), and an upper electrode (370) is formed on the dielectric layer. Hence, the diffusion barrier layer (355) is formed under the dielectric layer (360).

On the other hand, in the electrode structure recited in claims 1 and 3 of the present invention, the barrier metal layer is formed on the silicon-containing film provided on the gate insulating film. In other words, the barrier metal layer in claims 1 and 3 is provided

above the insulating film while the diffusion barrier layer in Agarwal '826 is provided under the insulating film. Hence, the arrangement of the electrode structure in claims 1 and 3 is opposite to that in Agarwal '826, and claims 1 and 3 are clearly distinguished from Agarwal '826.

Ouellet teaches an invention related to Al interconnects, and as shown in Fig. 15A, the invention includes the steps of forming an Al interconnect (4') on a substrate (2), for mixing a barrier layer (8) composed of non-stoichiometric TiN or Ti_2N on the Al interconnect (4'), and forming a dielectric layer (5) on the barrier layer (8). Hence, the barrier layer 8 is formed on the Al interconnect layer (4').

On the other hand, in the electrode structure recited in claims 1 and 3, the metal layer with a high melting point is formed on the barrier metal layer provided above the gate insulating film. In other words, the barrier metal layer in claims 1 and 3 of the present invention is provided under the metal layer with a high melting point, while the barrier layer in Ouellet is provided on the Al interconnect layer. Hence, the arrangement of the electrode structure in claims 1 and 3 is opposite to that of Ouellet, and claims 1 and 3 are clearly distinguished from Ouellet.

Nagasaka teaches an invention related to a barrier layer for contact electrode, and the invention includes the steps of forming a second TiN film (261B) (number Ti atom range from 50%-59%) on a contact area (42) of a Si device, forming a first TiN film (261A) that is rich in Ti and composed of TiN (number Ti atom range from 62%-75%) on the second TiN film (261B), and forming an electrode wiring (151) on the first TiN film (261A). Hence, the barrier metal layer (261) in Nagasaka has a two-layered structure, in which the upper-first barrier metal layer (261A) connected to the electrode wiring is a TiN layer rich in Ti, and the lower-second barrier metal layer (261B) connected to the Si is a TiN layer having substantially the same stoichiometric ratio.

On the other hand, in the two-layered structure of the barrier metal layer recited in claims 2 and 7, the lower-first barrier metal layer connected to the silicon-containing film is a TiN layer rich in Ti, and the upper-second barrier metal layer connected to the metal film with high melting point has a nitrogen composition higher than the stoichiometric ratio. In other words, in claims 2 and 7, the TiN layer rich in Ti is provided as the lower layer in the two-layered structure of the barrier metal layer, while in Nagasaka, the TiN layer rich in Ti is

provided as the upper layer in the two-layered structure of the barrier metal layer. Hence, the arrangement of the two-layered structure of the barrier metal layer in claims 2 and 7 is opposite to that of Nagasaka, and claims 2 and 7 are clearly distinguished from Nagasaka.

Ito teaches an invention related to a barrier layer for contact wiring, and the invention includes the steps of forming a Ti layer (185) within a contact hole (183) provided in a Si substrate (180), forming a second TiN_x layer (187) (x = N/Ti) on the Ti layer (185), forming a first TiN layer (186) on the second TiN_x layer (187), and forming a wiring conduct layer (182) on the first TiN layer (186). Ito further teaches that x is larger than 0 but smaller than 1 (see Fig. 3). Accordingly, since x = N/Ti and $0 < x < 1$, N < Ti. In other words, the barrier metal layer of Ito has a three-layered structure.

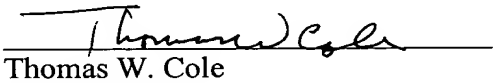
Further, according to Ito, the second TiNx layer (i.e., the middle layer) is a TiN layer rich in Ti (for example, Ti_2N layer), and Ito does not teach or suggest a TiN layer having a high nitrogen concentration as asserted by the Examiner. Therefore, the electrode structure and the film composition of the barrier metal layer in claims 2 and 7 are completely different from those of Ito, and the film composition of the barrier metal layer in claims 2 and 7 is distinguished from that of the barrier metal layer of Ito.

The requirements for establishing a *prima facie* case of obviousness, as detailed in MPEP § 2143 - 2143.03 (pages 2100-122 - 2100-136), are: first, there must be some suggestion or motivation, either in the reference themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the teachings; second, there must be a reasonable expectation of success; and, finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. As the cited prior art references are deficient, as discussed above, their combination in the §103(a) is be improper.

In view of the amendments and arguments set forth above, Applicants respectfully request reconsideration and withdrawal of all the pending rejections and objection.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with Applicant's representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby by expedited.

Respectfully submitted,



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